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relatively high voltages are applied to the drain and source (typical of a high-side application), the drain well region 12 will be completely depleted of its charge before the body buffer region 15 is depleted. This is due to the heavier doping of the body buffer region 15. This substantially prevents the occurrence of PT phenomena at relatively low voltages, which in turn enhances the performance of the structure of the invention under critical conditions of use.

## In the Claims:

Please cancel Claims 1 to 4.

Please add new Claims 5 to 25.

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- 5. A lateral diffused metal oxide semiconductor (LDMOS) integrated device comprising:
  - a semiconductor substrate;
- a drain region of a first conductivity type adjacent said semiconductor substrate and comprising a superficial buffer region being more heavily doped than adjacent portions of said drain region;
- a body region in said buffer region and having a second conductivity type; and
- a source region in said body region and having the first conductivity type.

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6. The LDMOS integrated device of Claim 5 wherein said drain region has a depth of about 1.5 to 4.5 micrometers.

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7. The LDMOS integrated device of Claim 5 wherein the portions of said drain region adjacent said superficial buffer region have a dopant concentration of about 2.5x1015 to  $2.5 \times 10^{16}$  atoms cm<sup>-3</sup>.

- The LDMOS integrated device of Claim 5 wherein said superficial buffer region has a depth of about 0.15 to 0.45 micrometers.
- The LDMOS integrated device of Claim 5 wherein said superficial buffer region has a dopant concentration of
- about  $5 \times 10^{16}$  to  $5 \times 10^{17}$  atoms cm<sup>-3</sup>.

  10. The LDMOS integrated device of Claim said body region has a depth of about 0.25 to 0.75 micrometers.

  11. The LDMOS integrated device of Claim 10. The LDMOS integrated device of Claim 5 wherein
  - The LDMOS integrated device of Claim 5 wherein said body region has a dopant concentration of about  $5x10^{17}$  to  $5 \times 10^{18}$  atoms cm<sup>-3</sup>.
  - The LDMOS integrated device of Claim 5 wherein said drain region is doped with phosphorous; and wherein said body region is doped with boron.
  - The LDMOS integrated device of Claim 5 wherein said drain region is doped with boron; and wherein said body region is doped with phosphorus.

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14. A lateral diffused metal oxide semiconductor (LDMOS) integrated device comprising:

a semiconductor substrate;

a drain region of a first conductivity type adjacent said semiconductor substrate and comprising a superficial buffer region being more heavily doped than adjacent portions of said drain region;

said superficial buffer region having a dopant concentration of about  $5 \times 10^{16}$  to  $5 \times 10^{17}$  atoms cm<sup>-3</sup> and the adjacent portions of said drain region having a dopant concentration of about  $2.5 \times 10^{16}$  to  $2.5 \times 10^{16}$  atoms cm<sup>-3</sup>;

a body region in said superficial buffer region and having a second conductivity type; and

a source region in said body region and having the first conductivity type.

15. The LDMOS integrated device of Claim 14 wherein said drain region has a depth of about 1.5 to 4.5 micrometers.

- 16. The LDMOS integrated device of Claim 14 wherein said buffer region has a depth of about 0.15 to 0.45 micrometers.
- 17. The LDMOS integrated device of Claim 14 wherein said body region has a depth of about 0.25 to 0.75 micrometers.
- 18. The LDMOS integrated device of Claim 14 wherein said body region has a dopant concentration of about  $5\times10^{17}$  to  $5\times10^{18}$  atoms cm<sup>-3</sup>.

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19. A method for making a lateral diffused metal oxide semiconductor (LDMOS) integrated device comprising:

forming a drain region having a first conductivity type adjacent a semiconductor substrate;

forming a superficial buffer region having the first conductivity type in the drain region so that the buffer region is more heavily doped than adjacent portions of the drain region;

forming a body region having a second conductivity type in the superficial buffer region; and

forming a source region having the first conductivity type in the body region.

20. The method of Claim 19 wherein the drain region  $\mu$  as a depth of about 1.5 to 4.5 micrometers.

- 21. The method of Claim 19 wherein the portions of the drain region adjacent said superficial buffer region have a dopant concentration of about  $2.5 \times 10^{15}$  to  $2.5 \times 10^{16}$  atoms cm<sup>-3</sup>.
- 22. The method of Claim 19 wherein the superficial buffer region has a depth of about 0.15 to 0.45 micrometers.
- 23. The method of Claim 19 wherein the superficial buffer region has a dopant concentration of about  $5 \times 10^{16}$  to  $5 \times 10^{17}$  atoms cm<sup>-3</sup>.
- $\dot{}$  24. The method of Claim 19 wherein the body region has a depth of about 0.25 to 0.75 micrometers.